# 74LCX139

## Low voltage CMOS
## Dual 2 to 4 decoder / demultiplexer

## Features

- 5V tolerant inputs
- High speed:
  - $t_{PD}$ = 6.2ns (Max) at $V_{CC}$ = 3V
- Power down protection on inputs and outputs
- Symmetrical output impedance:
  - $|I_{OH}| = I_{OL}$ = 24mA (Min) at $V_{CC}$ = 3V
- PCI bus levels guaranteed at 24mA
- Balanced propagation delays:
  - $t_{PLH} \cong t_{PHL}$
- Operating voltage range:
  - $V_{CC}$ (Opr) = 2.0V to 3.6V
- Pin and function compatible with 74 series 139
- Latch-up performance exceeds 500mA (JESD 17)
- ESD performance:
  - HBM > 2000V (MIL STD 883 method 3015); MM > 200V

SO-16 TSSOP16

## Description

The 74LCX139 is a low voltage CMOS dual 2 to 4 line Decoder / Demultiplexer fabricated with sub-micron silicon gate and double-layer metal wiring $C^2MOS$ technology.

It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for inputs.

The active low enable input can be used for gating or as a data input for demultiplexing applications. While the enable input is held high, all four outputs are high independently of the other inputs.

It has same speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

## Order codes

| Part number | Package | Packaging |
|---|---|---|
| 74LCX139MTR | SO-16 | Tape and reel |
| 74LCX139TTR | TSSOP16 | Tape and reel |

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# 1 Logic symbols and I/O equivalent circuit

**Figure 1. IEC logic symbols**

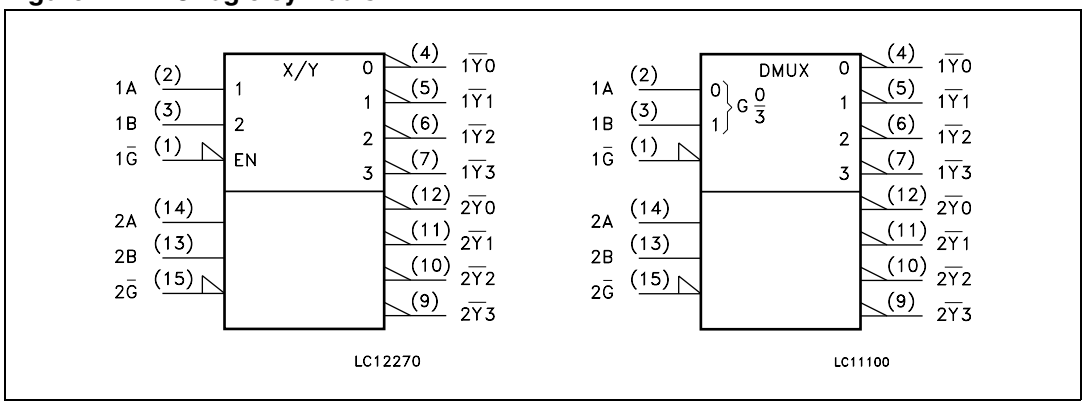
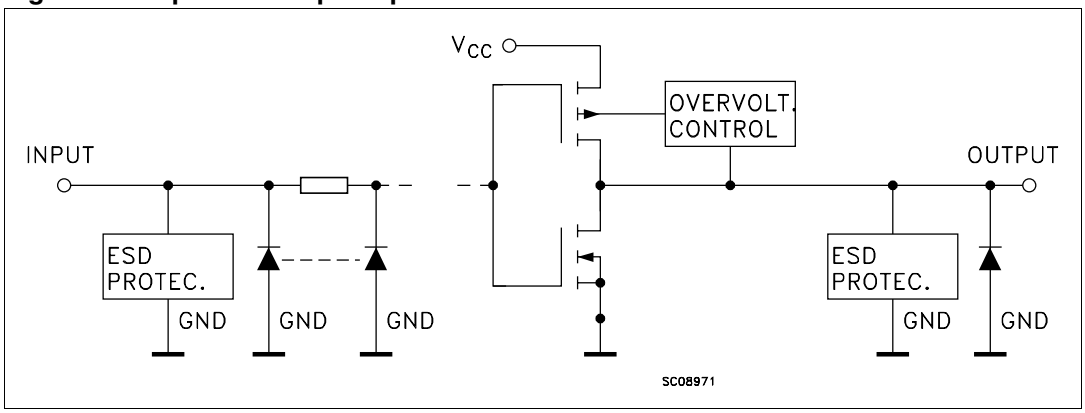


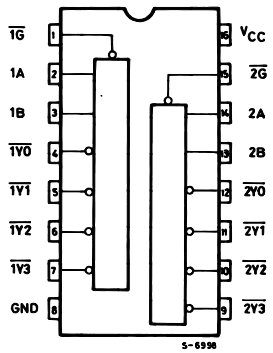

**Figure 2. Input and output equivalent circuit**



# 2 Pin settings

## 2.1 Pin connection

**Figure 3. Pin connection** (top through view)




## 2.2 Pin description

**Table 1. Pin description**

| Pin N° | Symbol | Name and function |
|---|---|---|
| 1, 15 | $1\overline{G}$, $2\overline{G}$ | Enable inputs |
| 2, 3 | 1A, 1B | Address inputs |
| 4, 5, 6, 7 | $1\overline{Y0}$ to $1\overline{Y3}$ | Outputs |
| 12, 11, 10, 9 | $2\overline{Y0}$ to $2\overline{Y3}$ | Outputs |
| 14, 13 | 2A, 2B | Address inputs |
| 8 | GND | Ground (0V) |
| 16 | $V_{CC}$ | Positive supply voltage |

## 2.3 Truth table

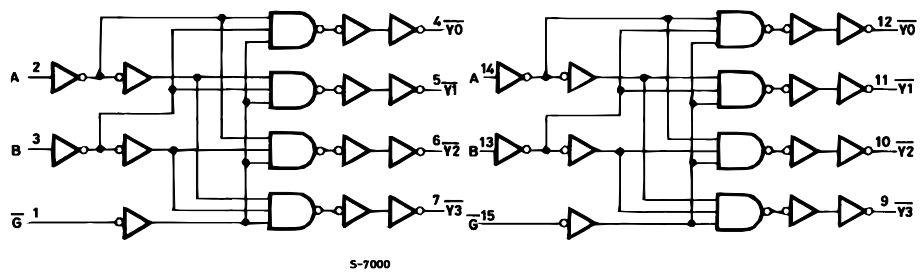
**Table 2. Truth table**

| Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| Enable | Select | | | | | |
| G | B | A | $\overline{Y0}$ | $\overline{Y1}$ | $\overline{Y2}$ | $\overline{Y3}$ |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

*Note: X : Do not care*

## 2.4 Logic diagram

**Figure 4. Logic diagram**




*Note: This logic diagram has not to be used to estimate propagation delays*

# 3 Maximum rating

stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. these are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. exposure to absolute maximum rating conditions for extended periods may affect device reliability. refer also to the STMicroelectronics sure program and other relevant quality documents.

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | -0.5 to +7.0 | V |
| $V_I$ | DC input voltage | -0.5 to +7.0 | V |
| $V_O$ | DC output voltage ($V_{CC}$ = 0V) | -0.5 to +7.0 | V |
| $V_O$ | DC output voltage (high or low state) (1) | -0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | DC input diode current | -50 | mA |
| $I_{OK}$ | DC output diode current (2) | -50 | mA |
| $I_O$ | DC output current | ±50 | mA |
| $I_{CC}$ | DC supply current per supply pin | ±100 | mA |
| $I_{GND}$ | DC ground current per supply pin | ±100 | mA |
| $T_{stg}$ | Storage temperature | -65 to +150 | °C |
| $T_L$ | Lead temperature (10 sec) | 300 | °C |

1. $I_O$ absolute maximum rating must be observed
2. $V_O$ < GND

## 3.1 Recommended operating conditions

**Table 4. Recommended operating conditions**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage (1) | 2.0 to 3.6 | V |
| $V_I$ | Input voltage | 0 to 5.5 | V |
| $V_O$ | Output voltage ($V_{CC}$ = 0V) | 0 to 5.5 | V |
| $V_O$ | Output voltage (high or low state) | 0 to $V_{CC}$ | V |
| $I_{OH}$, $I_{OL}$ | High or low level output current ($V_{CC}$ = 3.0 to 3.6V) | ±24 | mA |
| $I_{OH}$, $I_{OL}$ | High or low level output current ($V_{CC}$ = 2.7V) | ±12 | mA |
| $T_{op}$ | Operating temperature | -40 to 85 | °C |
| dt/dv | Input rise and fall time (2) | 0 to 10 | ns/V |

1. Truth table guaranteed: 1.5V to 3.6V
2. $V_{IN}$ from 0.8V to 2V at $V_{CC}$ = 3.0V

# 4 Electrical characteristics

**Table 5. DC specifications**

| Symbol | Parameter | Test condition | | Value | | Unit |
|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | -40 to 85°C | | |
| | | | | Min | Max | |
| $V_{IH}$ | High level input voltage | 2.7 to 3.6 | | 2.0 | | V |
| $V_{IL}$ | Low level input voltage | | | | 0.8 | V |
| $V_{OH}$ | High level output voltage | 2.7 to 3.6 | $I_O$=-100 µA | $V_{CC}$-0.2 | | V |
| | | 2.7 | $I_O$=-12 mA | 2.2 | | |
| | | 3.0 | $I_O$=-18 mA | 2.4 | | |
| | | | $I_O$=-24 mA | 2.2 | | |
| $V_{OL}$ | Low level output voltage | 2.7 to 3.6 | $I_O$=100 µA | | 0.2 | V |
| | | 2.7 | $I_O$=12 mA | | 0.4 | |
| | | 3.0 | $I_O$=16 mA | | 0.4 | |
| | | | $I_O$=24 mA | | 0.55 | |
| $I_I$ | Input leakage current | 2.7 to 3.6 | $V_I$ = 0 to 5.5V | | ±5 | µA |
| $I_{off}$ | Power OFF leakage current | 0 | $V_I$ or $V_O$ = 5.5V | | 10 | µA |
| $I_{CC}$ | Quiescent supply current | 2.7 to 3.6 | $V_I$ = $V_{CC}$ or GND | | 10 | µA |
| | | | $V_I$ or $V_O$= 3.6 to 5.5V | | ±10 | |
| $\Delta I_{CC}$ | I incr. per Input | 2.7 to 3.6 | $V_{IH}$ = $V_{CC}$ - 0.6V | | 500 | µA |

**Table 6. Dynamic switching characteristics**

| Symbol | Parameter | Test condition | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | $T_A$ = 25 °C | | | |
| | | | | Min | Typ | Max | |
| $V_{OLP}$ | Dynamic low level quiet output (1) | 3.3 | $C_L$ = 50pF<br>$V_{IL}$ = 0V, $V_{IH}$ = 3.3V | | 0.8 | | V |
| $V_{OLV}$ | | | | | -0.8 | | |

1. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

### Table 7. AC electrical characteristics

| Symbol | Parameter | Test condition | | | | Value | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | $C_L$ (pF) | $R_L$ (Ω) | $t_s = t_r$ (ns) | -40 to 85 °C | | |
| | | | | | | Min | Max | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time A, B to $\overline{Y}$ | 2.7 | 50 | 500 | 2.5 | | 7.3 | ns |
| | | 3.0 to 3.6 | | | | 1.0 | 6.2 | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time $\overline{G}$ to $\overline{Y}$ | 2.7 | 50 | 500 | 2.5 | | 5.8 | ns |
| | | 3.0 to 3.6 | | | | 1.0 | 5.3 | |
| $t_{OSLH}$ $t_{OSHL}$ | Output To Output Skew Time (1) (2) | 3.0 to 3.6 | 50 | 500 | 2.5 | | 1.0 | ns |

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = | t_{PLHm} - t_{PLHn} |$, $t_{OSHL} = | t_{PHLm} - t_{PHLn} |$)
2. Parameter guaranteed by design

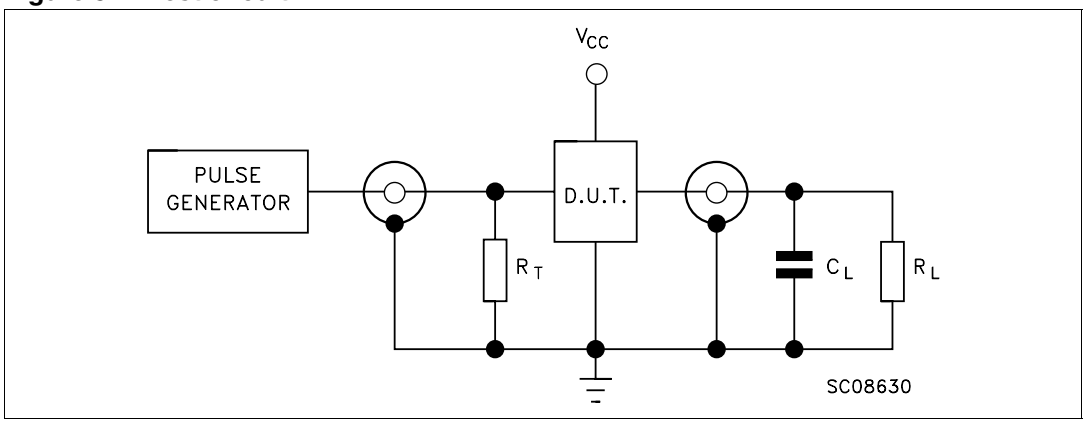
### Table 8. Capacitive characteristics

| Symbol | Parameter | Test condition | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | $T_A$ = 25 °C | | | |
| | | | | Min | Typ | Max | |
| $C_{IN}$ | Input capacitance | 3.3 | $V_{IN}$ = 0 to $V_{CC}$ | | 6 | | pF |
| $C_{PD}$ | Power dissipation capacitance (1) | 3.3 | $f_{IN}$ = 10MHz<br>$V_{IN}$ = 0 or $V_{CC}$ | | 26 | | pF |

1. $C_{PD}$ is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

# 5 Test circuit

**Figure 5. Test circuit**




*$C_L$ = 50pF or equivalent (includes jig and probe capacitance)*

*$R_L$ = 500Ω or equivalent*

*$R_T$ = $Z_{OUT}$ of pulse generator (typically 50Ω)*

# 6 Waveforms

**Figure 6. Propagation delay for inverting outputs** (f = 1MHz; 50% duty cycle)

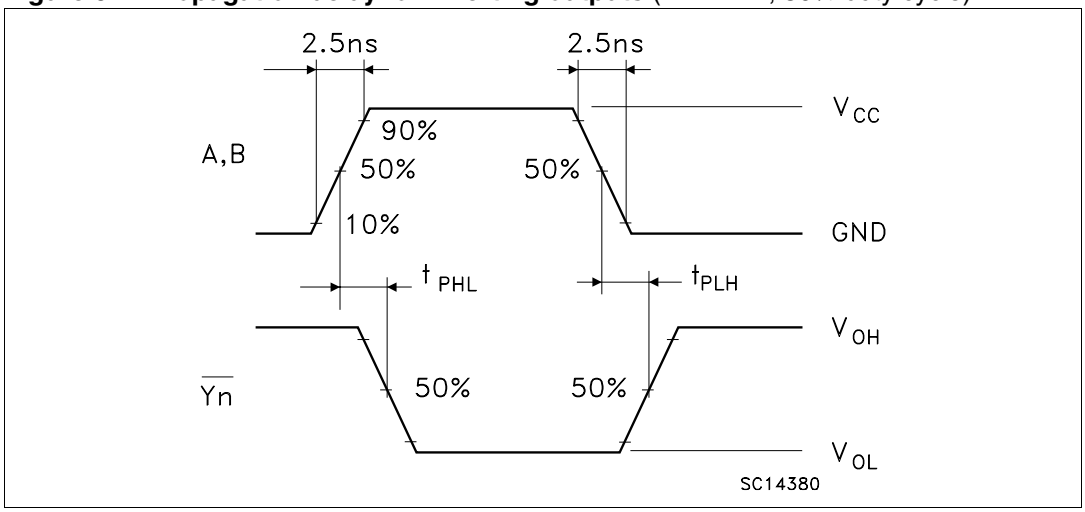
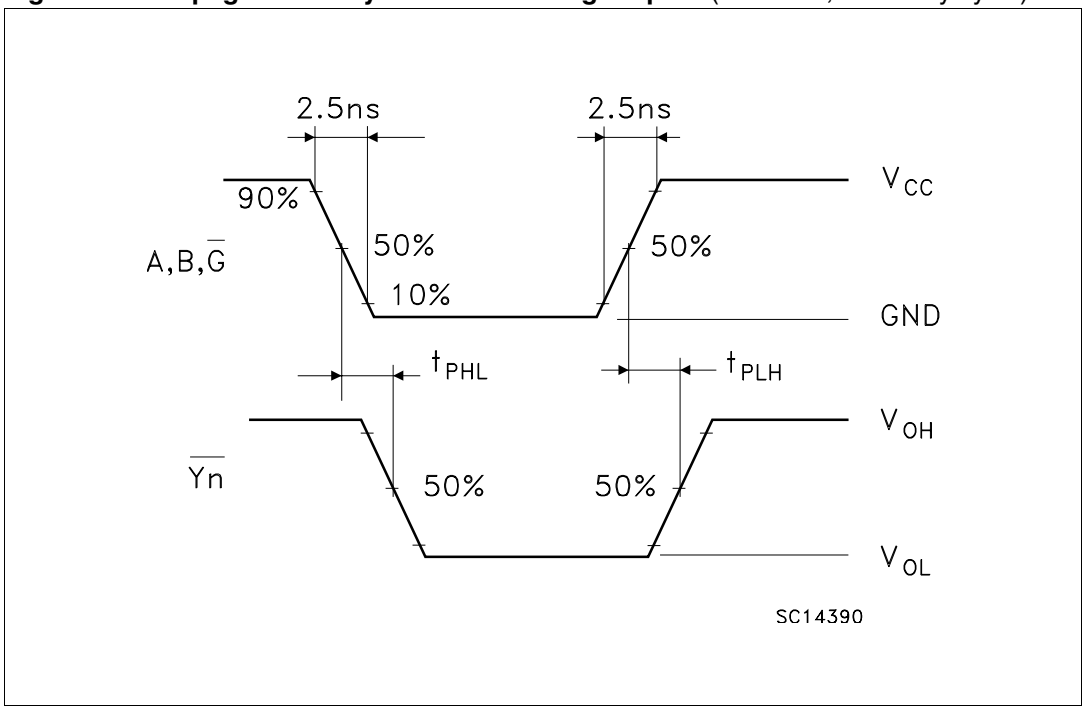



**Figure 7. Propagation delay for non-inverting outputs** (f = 1MHz; 50% duty cycle)

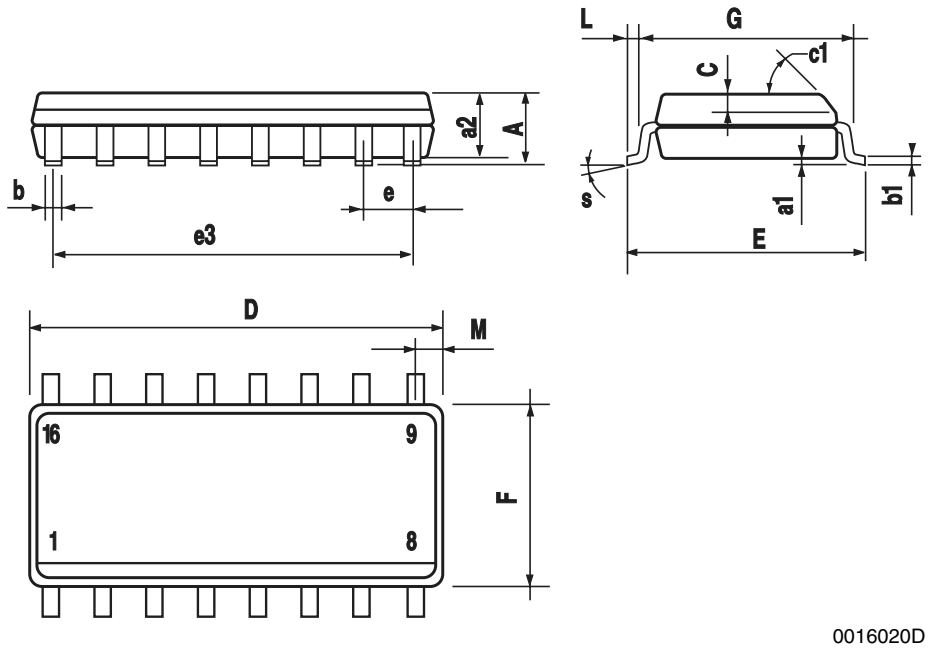


# 7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

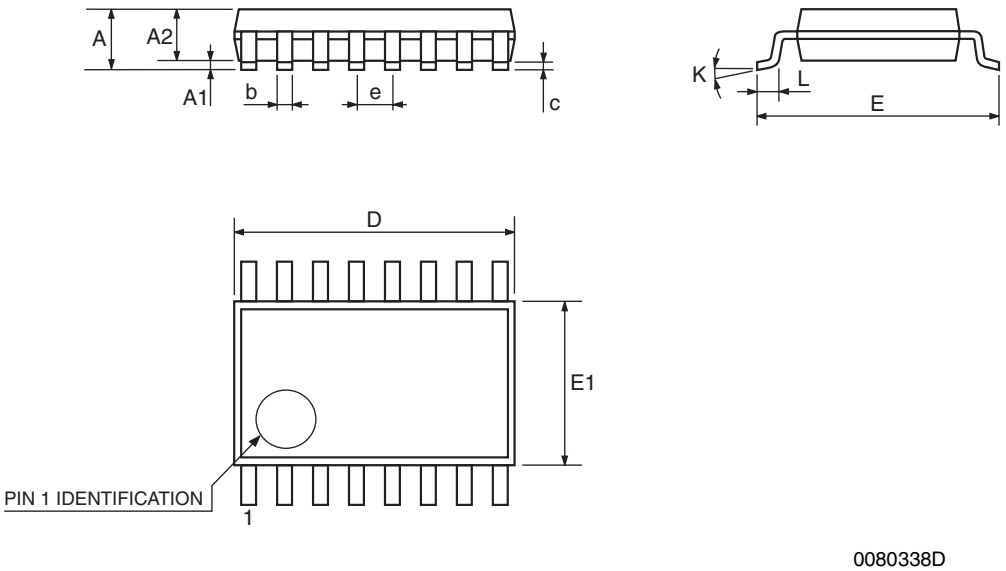
## SO-16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.068 |
| a1 | 0.1 | | 0.25 | 0.004 | | 0.010 |
| a2 | | | 1.64 | | | 0.063 |
| b | 0.35 | | 0.46 | 0.013 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | | 0.5 | | | 0.019 | |
| c1 | 45° (typ.) | | | | | |
| D | 9.8 | | 10 | 0.385 | | 0.393 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 8.89 | | | 0.350 | |
| F | 3.8 | | 4.0 | 0.149 | | 0.157 |
| G | 4.6 | | 5.3 | 0.181 | | 0.208 |
| L | 0.5 | | 1.27 | 0.019 | | 0.050 |
| M | | | 0.62 | | | 0.024 |
| S | 8° (max.) | | | | | |



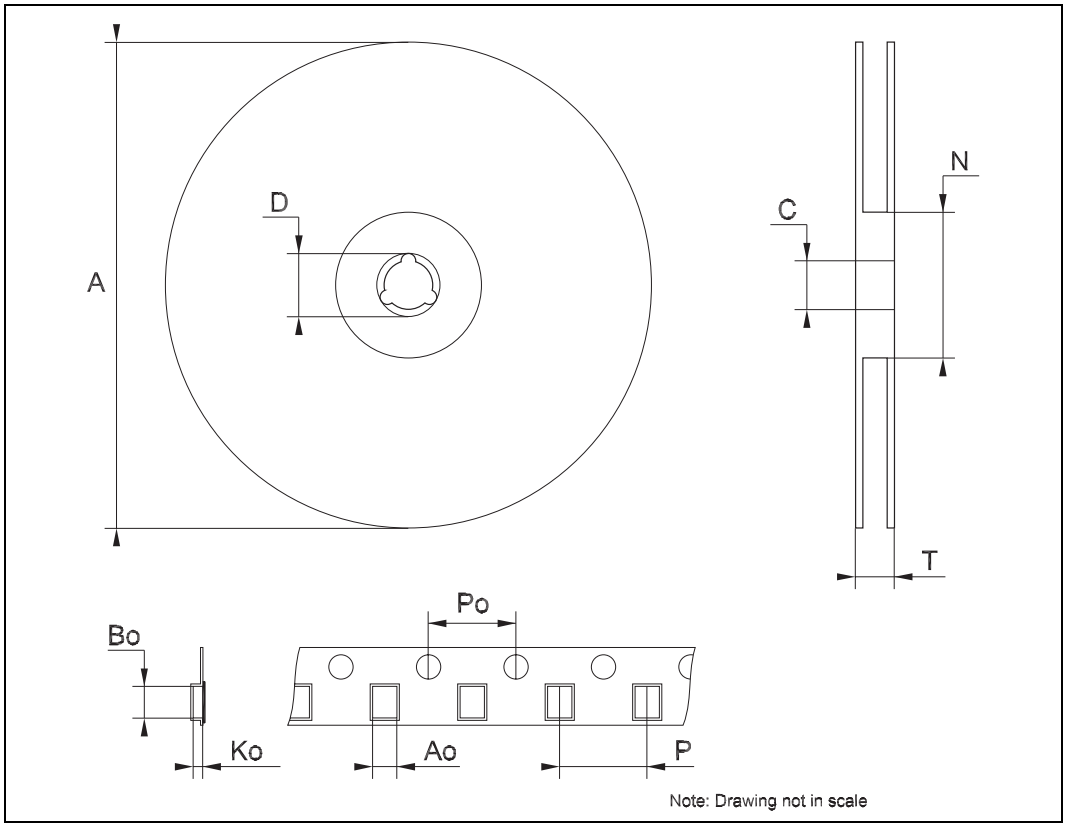
## TSSOP16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.2 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.8 | 1 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0079 |
| D | 4.9 | 5 | 5.1 | 0.193 | 0.197 | 0.201 |
| E | 6.2 | 6.4 | 6.6 | 0.244 | 0.252 | 0.260 |
| E1 | 4.3 | 4.4 | 4.48 | 0.169 | 0.173 | 0.176 |
| e | | 0.65 BSC | | | 0.0256 BSC | |
| K | 0° | | 8° | 0° | | 8° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |



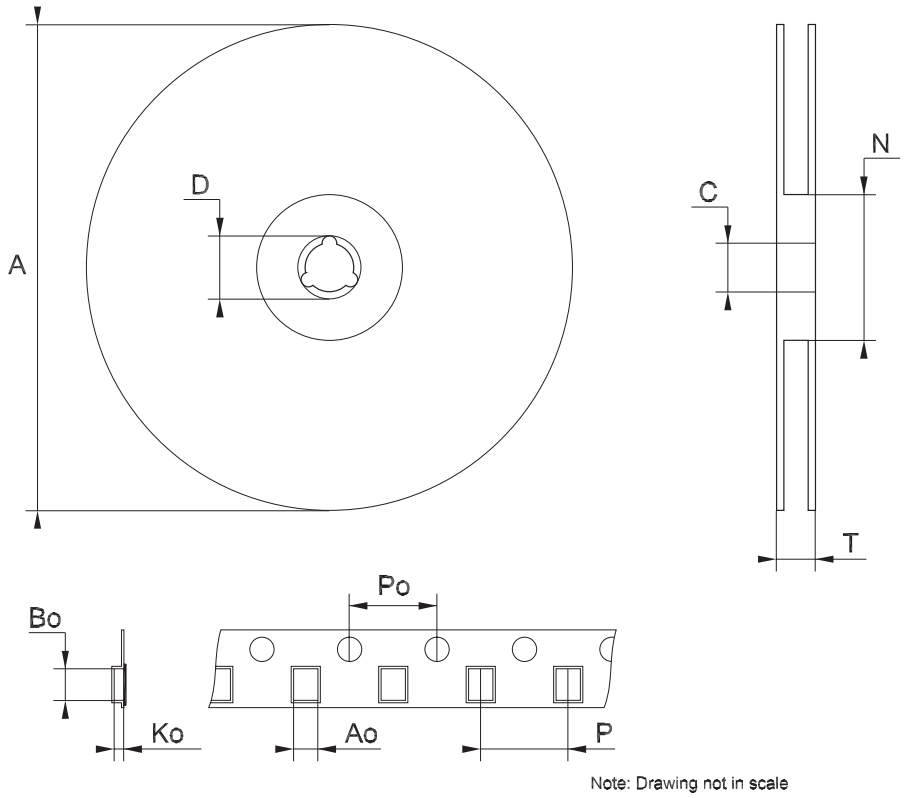
## Tape & Reel SO-16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 22.4 | | | 0.882 |
| Ao | 6.45 | | 6.65 | 0.254 | | 0.262 |
| Bo | 10.3 | | 10.5 | 0.406 | | 0.414 |
| Ko | 2.1 | | 2.3 | 0.082 | | 0.090 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 7.9 | | 8.1 | 0.311 | | 0.319 |



## Tape & Reel TSSOP16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 22.4 | | | 0.882 |
| Ao | 6.7 | | 6.9 | 0.264 | | 0.272 |
| Bo | 5.3 | | 5.5 | 0.209 | | 0.217 |
| Ko | 1.6 | | 1.8 | 0.063 | | 0.071 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 7.9 | | 8.1 | 0.311 | | 0.319 |



# 8 Revision history

**Table 9. Revision history**

| Date | Revision | Changes |
|---|---|---|
| 15-Sep-2004 | 3 | Ordering Codes Revision - pag. 1. |
| 27-Jul-2006 | 4 | New template, temperature ranges updated |

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